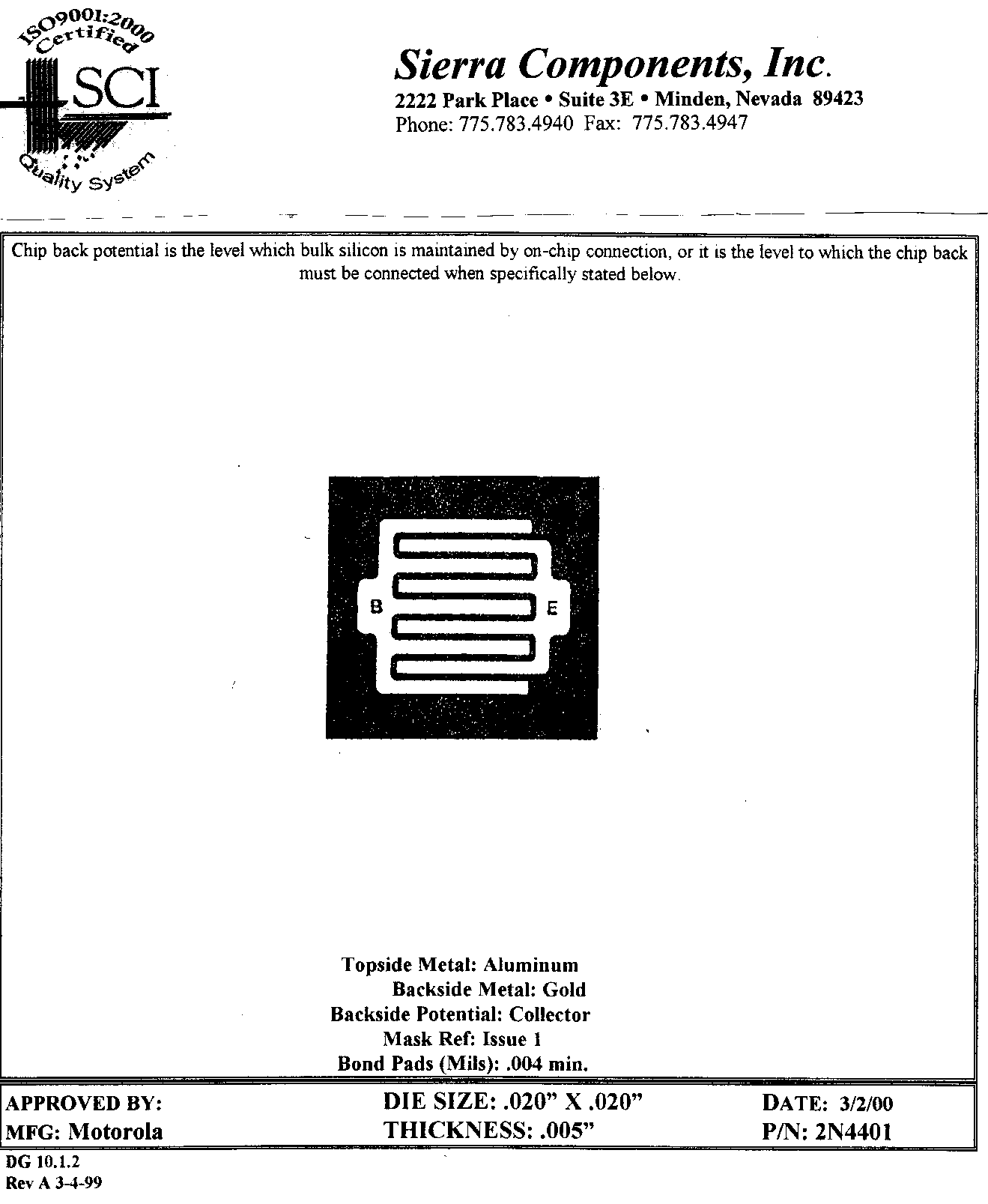
Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**.020”**



**.020”**

**Top Material: Al**

**Backside Material: Au**

**Bond Pad Size: .0028” x .006” min.**

**Backside Potential: COLLECTOR**

**Mask Ref: SL333**

**APPROVED BY: DK DIE SIZE .020” X .020” DATE: 3/28/22**

**MFG: MOTOROLA THICKNESS .005” P/N: 2N4401**

**DG 10.1.2**

#### Rev B, 7/19/02